



Storm-1 Stream Processors

Parallel Processing.
Made Simple.



SP16-G160 Product Brief

A member of SPI's groundbreaking Storm-1 family, the SP16-G160 device is designed for high-performance signal processing, video, and imaging applications. Based on the latest developments in stream processing, SP16-G160 delivers industry-leading DSP performance leveraged by a simple C programming model that harnesses parallelism.

Stream Processing: Today's State-of-the-art in DSP Technology

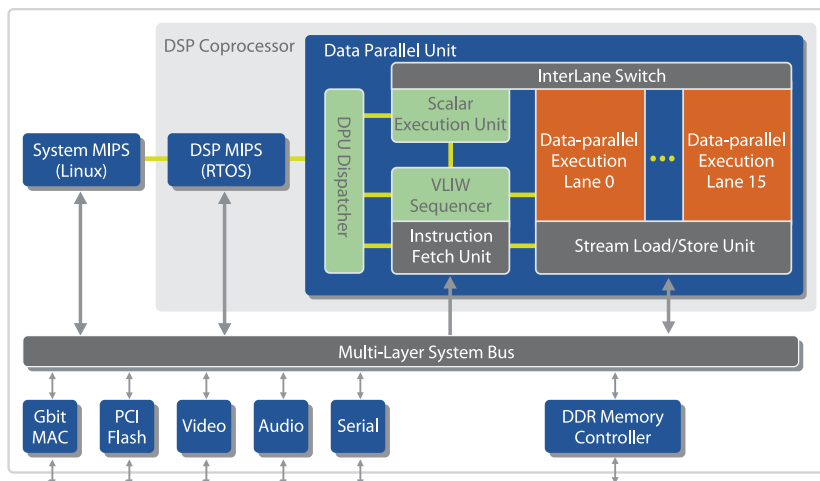
Data bandwidth and data movement, not arithmetic, is what matters in modern computer systems. Stream processing is an architecture and programming model designed from ground up to optimize bandwidth using compiler-managed memory hierarchy to both unleash and make parallel processing easy to use.

Based on established DSP methods, the C programming model allows the user to define compute-intensive kernel functions that process and produce finite batches of data records, called streams. SPI tools exploit this to optimize allocation of streams in on-chip memory and setup DMAs driven by runtime dependencies.

In the execution model, main threads run on the DSP MIPS and make kernel function calls to the Data Parallel Unit, where one kernel function at a time processes its streams across the lanes. Each lane has 5 ALUs fed by an explicitly managed memory hierarchy to deliver sustained, predictable performance.

With a robust programming and development tools approach combined with a bandwidth-driven and scalable architecture, SPI's platform efficiently harnesses parallel processing for embedded systems, empowering users with the flexibility of software and a less engineering-intensive alternative to FPGAs, ASICs and multi-DSP designs.

SP16-G160 Block Diagram



Target Applications

- Multi-channel video/audio decode, encode and transcoding
- HD video conferencing endpoints and MCUs
- Video surveillance DVRs, encoders and intelligent video analytics
- Print/copy/scan image processing for mid to high-end

Features and Benefits

- A new level of performance for increased density and reduced cost
- Programmable DSP platform supporting multiple standards and differentiation via software
- Inherently load-balanced bandwidth-optimized data-parallel stream processing architecture
- User-friendly ANSI C programming for control and DSP code reduces effort and time to market
- Development tools that manage memory and DMA for a predictable path to production code
- Libraries and SPI ecosystem accelerate development
 - Filters, transforms
 - Codecs, analytics, scan/print processing
 - E.g. H.264, MPEG-4, VC-1, object tracking, labeling

Performance Snapshot

- 16x16 SAD at 120 MSADs/s
- 8x8 DCT at 6 Gpixels/s
- 7x7 2-D FIR at 1.3 Gpixels/s
- HD 1080p30 H.264 encode
- 8 x D1 MPEG-4 encode

Specification Summary

- SoC with System CPU, DSP subsystem and rich I/O
- DSP subsystem based on stream processing
 - 160 GOPS or 80,000 MMACS (16-bit)
 - <0.1mW/MMAC energy efficiency
 - Data Parallel Unit with 16 lanes and 5 individual ALUs per lane in a 12-way VLIW, with each ALU capable of 4x8-/2x16-/1x32-bit operations/cycle, including MACs
 - 250 MHz MIPS 4KEc™ core dedicated for DSP threads
- SPI Stream Processor™ architecture
 - C programming model with tools-automated memory management and DMA
 - Inherently load-balanced massively parallel execution
 - Memory hierarchy and available bandwidth tuned to the locality of compute-intensive DSP applications
 - Flexible data-parallelism with support for conditionals and full inter-lane crossbar
- 250 MHz MIPS 4KEc™ core dedicated for System and I/O
- On-chip memory
 - 256 KB Lane Register Files (16 KB per lane)
 - 19 KB Operand Register Files (304 words per lane)
 - 96 KB VLIW instruction memory
 - 2 x 16/16 KB MIPS data/instruction caches
- External memory interface
 - 16-/32-/64-/128-bit DDR1/DDR2, 400 MHz data rate
 - 8-bit PIO (flash, SRAM)
- I/O interfaces
 - Ethernet - 10/100/1000 Mbit controller (GMII/MII)
 - PCI - 33/66 MHz, 32-bit, PCI 2.2 master/agent
 - 20 GBytes/s interconnect bus with 28 DMA channels
 - StreamIO™ - 108 configurable high-speed in/output pins for video, sensor and data
 - 9/6 SD/HD video ports of 8/10 or 16/20-bit BT.656, BT.1120.5, SMPTE260M/274M/296M
 - 24-bit RGB in/out and 16-bit Bayer CMOS input
 - Nine I2S, four I2C, two SSP/SPI/Microwire, three UARTs and up to 64 GPIO pins (muxed)
- Four 32-bit timer outputs for realtime clock, watchdog and PWM
- Multiple boot and debug modes
- Hardware support for trace and statistical profiling
- IEEE 1149.1 JTAG and EJTAG interfaces
- Power management and sleep modes with clock gating at ALU, lane and DPU levels
- Four programmable PLL clock domains
- Package/Voltage/Process
 - 896-pin, 31 x 31mm PBGA, 1 mm pitch
 - Core nominal voltage – 1.1V
 - Memory voltage - 1.8V / 2.5V (DDR2 / DDR1)
 - I/O voltages – 3.3V
 - 130 nm TSMC



Development Tools

- RapiDev™ Tools Suite supporting Windows/Cygwin and Linux environments
- Cross development tools (gcc 3.4.4), board support package with device drivers and source code for Linux kernel (2.6.13) distribution and U-Boot
- Optimizing C compiler that automates on-chip memory management and DMA scheduling
- Fast Functional Debugging library for MS Visual Studio and GDB
- Cycle-accurate Target Code Simulator with source-level debugging, stream and kernel level visualization
- Royalty-free Linux for System MIPS and Nucleus RTOS for DSP MIPS
- Multi-tasking DSP application and MIPS messaging framework
- Storm-1 DevKit development board



Stream Processors, Inc.

www.streamprocessors.com

455 DeGuigne Drive
 Sunnyvale, CA 94085-3890 USA
T +1 408.616.3338
F +1 408.616.3337

Learn more: Visit www.streamprocessors.com

©2007 Stream Processors, Inc. All rights reserved. This document contains advance information on SPI products that are in development, sampling or initial production phases. The information and specifications contained herein are subject to change at the discretion of Stream Processors, Inc.
 Document number: PB-SP16-G160-001 (April 2007)